What is claimed is:

1. A telecommunication system comprising:

a telephone headset;

a headset adapter coupled to the telephone headset and having an accessory interface bus for transmitting and receiving communications packets; and

an accessory for the telephone headset coupled to the accessory interface bus of the headset adapter, wherein the accessory can be directly controlled or monitored by the headset adapter via the transmission of communications packets between the accessory and the headset adapter over the accessory interface bus.

2. The system of claim 1, wherein the accessory interface bus includes at least one bi-directional signaling line for transmitting and receiving the communications packets between the accessory and the headset adapter in order to control or monitor the accessory.

3. The system of claim 1, wherein the accessory interface bus further includes:

a high voltage rail;

a low voltage rail; and

at least one bi-directional signaling line for transmitting and receiving communications packets between the accessory and the headset adapter in order to control or monitor the accessory.

4. The system of claim 1, wherein each communications packet includes a synch pulse which defines a transmission rate for the communications packet.

5. The system of claim 4, wherein the synch pulse includes a rate bit having a bit period which defines the transmission rate for the communications packet.

6. The system of claim 5, wherein the rate bit includes a rising edge and a falling edge within the bit period, and further wherein a duration of time between the rising edge and the falling edge is used to determine the bit period which is inversely related to the transmission rate of the communications packet.

7. The system of claim 5, wherein the synch pulse holds the accessory bus at a predetermined level for a predetermined amount of time before the rate bit of the communications packet is transmitted over the accessory bus thereby preventing collision between communications packets.

8. The system of claim 7, wherein the synch pulse holds the accessory interface bus to a low voltage value for at least two bit periods before the rate bit is transmitted in order to prevent collision between communications packets.

9. The system of claim 1, wherein each communications packet includes a source address indicating a bus address of the source of the communications packet, a destination address indicating a bus address of the destination of the communications packet, and a command or data.

10. The system of claim 9, wherein each communications packet further includes a checksum for detecting errors in transmission of the communications packet.

11. The system of claim 1, wherein each communications packet includes a plurality of bits with each bit in the plurality of bits having an assigned value of zero

or one, and further wherein each bit includes a first signal portion having a first logic level and a second signal portion having a second logic level and the assigned value of zero or one is assigned to each bit based upon a duration of either the first signal portion or the second signal portion.

12. The system of claim 11, wherein if the duration of the at least one portion falls within a first range the bit is assigned a value of zero and if the duration of the at least one portion falls within a second range, the bit is assigned a value of one.

13. The system of claim 11 wherein each bit in the plurality of bits has a rising edge and a falling edge, and the rising edge and the falling edge are used to synchronize transmission of the communications packet after each bit is transmitted.

14. The system of claim 1, wherein the headset adapter includes a micro-controller coupled to the interface bus, the micro-controller controlling and monitoring the accessory through the transmission and reception of communications packets between the micro-controller and the accessory via the interface bus.

15. An adapter base for a telecommunications headset comprising:

an interface bus; and

a micro-controller coupled to the interface bus, for controlling and monitoring at least one accessory to the telecommunications headset which is coupled to the interface bus, wherein the micro-controller controls and monitors the accessory through the bi-directional transmission of communications packets between the micro-controller and the accessory via the interface bus.

16. The adapter base of claim 15, wherein the interface bus includes a high voltage rail, a low voltage rail, and a bi-directional signaling line for transmitting the communications packets back and forth over the interface bus between the micro-controller and the accessory.

17. The adapter base of claim 15, wherein each communications packet includes a synch pulse which defines a rate of transmission for that communications packet.

18. The adapter base of claim 17, wherein the synch pulse includes a rate bit having a bit period which defines the transmission rate for the communications packet.

19. The adapter base of claim 18, wherein the rate bit includes a rising edge and a falling edge within the bit period, and further wherein a duration of time between the rising edge and the falling edge is used to determine the bit period which is inversely related to the transmission rate for the communications packet.

20. The adapter base of claim 17, wherein the synch pulse holds the accessory bus at a predetermined level for a predetermined amount of time before each communications packet is transmitted over the accessory bus in order to gain bus control.

21. The adapter base of claim 15, wherein each communications packet includes a source address indicating a bus address of the source of the communications packet, a destination address indicating a bus address of the destination of the communications packet, and a command or data.

22. The adapter base of claim 21, wherein each communications packet further includes a checksum for detecting errors in transmission of the communications packet.

23. The adapter base of claim 15, wherein each communications packet includes a plurality of bits, with each bit in the plurality of bits having an assigned value of zero or one, and further wherein each bit includes a first signal portion having a first logic level and a second signal portion having a second logic level and the assigned value of zero or one is assigned to each bit is based upon a duration of either the first signal portion or the second signal portion.

24. The adapter base of claim 23, wherein if the duration of the at least one portion falls within a first range the bit is assigned a value of zero and if the duration of the at least one portion falls within a second range, the bit is assigned a value of one.

25. The adapter base of claim 23, wherein each bit in the plurality of bits has a rising edge and a falling edge, and the rising edge and the falling edge are used to synchronize transmission of the communications packet after each bit is transmitted.

26. A telephone headset accessories interface bus for controlling and monitoring a telephone headset accessory which is coupled to the interface bus, the telephone headset accessories interface bus capable of transmitting and receiving a plurality of communications packets for controlling or monitoring the telephone headset accessory.

27. The telephone headset accessories interface bus of claim 25, comprising:

a high voltage,

a low voltage rail, and

at least one bidirectional signaling line for transmitting and receiving the plurality of communications packets between a headset adapter and the telephone headset accessory, wherein the communications packets are used to control or monitor the telephone headset accessory.

28. The telephone headset accessories interface bus of claim 26, wherein each communications packet in the plurality of communications packets further includes a synch pulse which defines a rate of transmission at which the communications packet is transmitted.

29. The telephone headset accessories interface bus of claim 28, wherein the synch pulse includes a rate bit having a bit period which defines the transmission rate for the communications packet.

30. The telephone headset accessories interface bus of claim 26, wherein each communications packet further includes a source address indicating a bus address of a source of the communications packet, a destination address byte indicating a bus address of a destination of the communications packet, and a command or data.

31. The telephone headset accessories interface bus of claim 30, wherein each communications packet further includes a checksum for detecting errors in transmission of the communications packet.

32. The telephone headset accessories interface bus of claim 26, wherein each communications packet includes a plurality of bits with each bit having a high bit portion and a low bit portion such that each bit has a rising edge and a falling edge within a single bit period, and further wherein the rising edge and the falling edge are used to synchronize transmission of the single communications packet after each bit is transmitted.

33. An interface bus that transmits and receives a plurality of communications packets between a headset adapter and a headset accessory, thereby allowing the headset adapter to control, monitor and test the headset accessory.

34. The interface bus of claim 33, wherein each communications packet in the plurality of communications packet has a synch pulse for defining a transmission rate for the communications packet.

35. The interface bus of claim 34, wherein the synch pulse includes a rate bit having a bit period which defines the transmission rate for the communications packet.

36. The interface bus of claim 33, wherein each communications packet includes a source address indicating a bus address of a source of the communications packet, a destination address indicating a bus address of a destination of the communications packet, and a command or data.

37. The interface bus of claim 36, wherein each communications packet further includes a checksum for detecting errors in transmission of the communications packet.

38. The interface bus of claim 33, wherein each communications packet includes a plurality of bits with each bit having an assigned value of one or zero, and further wherein each bit includes a high bit portion and a low bit portion, with the duration of at least one bit portion determining the value of one or zero which is assigned to the bit such that if the duration of such portion falls within a first range the bit is assigned a value of zero and if the duration of such portion falls within a second range, the bit is assigned a value of one.

39. The interface bus of claim 38, wherein each bit in the plurality of bits has a rising edge and a falling edge within a single bit period, and further wherein the rising edge and the falling edge can be used to synchronize transmission of the communications packet after each bit period.

40. A method for controlling or monitoring an accessory to a telecommunications headset using a headset adapter base and an interface bus, the method comprising:

detecting whether an accessory is coupled to the interface bus; and

transmitting a command or status request signal from the adapter base over the interface bus and to the accessory in order to control or monitor operation of the accessory.

41. The method of claim 40, wherein the command or status request signal is a communications packet having a synch pulse for defining a transmission rate of the communications packet, such that the adapter base communicates with the accessory at its own transmission rate.

42. The method of claim 41, wherein the communications packet further includes a source address indicating a bus address of the adapter base and a destination address indicating a bus address of the accessory.

43. The method of claim 40 further comprising:

detecting any errors in the transmission of the command or status request signal from the adapter base over the interface bus.

44. The method of claim 42, wherein the communications packet further includes a checksum for detecting errors in transmission of the communications packet.

45. The method of claim 40 further comprising:

receiving a response signal from the accessory returning information on the current status of the accessory when a status request signal is transmitted.

46. The method of claim 45, wherein the response signal is a communications packet having a synch pulse for defining a transmission rate of the communications packet, such that the accessory communicates with the adapter base at its own transmission rate.

47. The method of claim 45, wherein the communications packet further includes a source address indicating a bus address of the accessory and a destination address indicating a bus address of the adapter base.

48. The method of claim 46, wherein the communications packet further includes a checksum for detecting errors in transmission of the communications packet from the accessory to the adapter base.

49. The method of claim 40, further comprising:

holding the interface bus at a predetermined voltage level for a predetermined amount of time after a command signal is

transmitted to the accessory, in order to allow the accessory to acknowledge receipt of the command signal.

50. The method of claim 41, wherein the communications packet includes a plurality of bits with each bit having a high bit portion and a low bit portion such that each bit has a rising edge and a falling edge within a single bit period, and further wherein the rising edge and the falling edge are be used to synchronize transmission of the command or status request signal after each bit is transmitted.

51. A data packet transmitted over an accessory interface bus having a number of devices coupled thereto for controlling, monitoring or testing the operations of a headset accessory coupled to the interface bus, the data packet comprising:

a synch pulse having a rate bit that defines a rate at which the data packet is being transmitted;

a source address byte that represents a bus address of a device from which the data packet was transmitted; and

a destination address byte that represents a bus address of the headset accessory to which the data packet is being transmitted.

52. The data packet of claim 51, further comprising a checksum byte for detecting errors in transmission of the data packet.

53. The data packet of claim 51, further comprising a plurality of bits with each bit having an assigned value of one or zero, wherein each bit has a high bit portion and a low bit portion within a single bit period, with the duration of at least one bit portion determining the value of one or zero which is assigned to the bit such that if the duration of the at least one bit portion falls within a first range the bit

is assigned a value of zero and if the duration of the at least one bit portion falls within a second range, the bit is assigned a value of one.

54. The data packet of claim 53 wherein each bit in the plurality of bits has a rising edge and a falling edge within the single bit period, said rising edge and falling edge used to synchronize transmission of the data packet after each bit is transmitted.

55. A method for assigning a bit value of one or zero to a data bit having a high portion and a low portion within a single bit period, the method comprising the steps of:

receiving the data bit;

measuring a width of either the high portion or the low portion; and

assigning a bit value of one to the data bit if the width measured falls within a first predetermined range or assigning a bit value of zero to the data bit if the width measured falls within a second predetermined range.

56. A communications protocol for a telephone headset accessories interface bus comprising a plurality of commands to control, monitor, or identify any one of a plurality of accessories coupled to the interface bus.

57. The communications protocol of claim 56, wherein the plurality of commands include common commands for controlling and monitoring any one of the plurality of accessories and accessory specific commands for controlling and monitoring a specific accessory in the plurality of accessories.

58. The communications protocol of claim 57 wherein the common commands include:

a command for polling the interface bus and detecting each of the plurality of accessories; and

a command for resetting each of the plurality of accessories;

59. The communications protocol of claim 57 wherein the common commands include:

a command for requesting a firmware version number from each accessory in the plurality of accessories.

60. The communications protocol of claim 57 wherein the accessory specific commands include:

a command for turning the specific accessory on or off;

a command for resetting the specific accessory; and

a command for requesting the status of the specific accessory.

61. The communications protocol of claim 57 wherein the accessory specific commands include a command for simulating a button press of the specific accessory.

62. The communications protocol of claim 57 wherein the accessory specific commands include:

a command for writing data to a memory within the specific accessory; and

a command for reading data from a memory within the specific accessory.

63. A combination comprising:

an interface bus having a telephone headset adapter base and a plurality of accessories for the headset adapter base coupled to the interface bus, and

a communications protocol for controlling and monitoring operations of the headset adapter base and the plurality of accessories, the communications protocol including at least one command selected from the group of commands consisting of:

a command for turning an accessory on or off;

a command for polling the interface bus in order to determine what accessories are coupled to the interface bus;

a command for simulating operations as if a button, a switch or a dial on an accessory had been activated;

a command for simulating operations as if a button, a switch of a dial on the headset adapter base had been activated;

a command for resetting an accessory;

a command for determining the status of an accessory;

a command for reading from or writing to a memory structure within an accessory; and

a command for determining the identity and version of each accessory.

64. The combination of claim 63, wherein the communications protocol includes a data packet which is transmitted over the interface bus for controlling and monitoring operations of the headset adapter base and the plurality of accessories coupled to the interface bus, the data packet comprising:

a synch pulse having a rate bit which defines a speed at which the data packet is transmitted;

a source address byte which represents a bus address where the data packet was transmitted from; and

a destination address byte which represents a bus address where the data packet is being transmitted.

65. The combination of claim 64, wherein the data packet further includes a checksum for detecting errors in transmission of the communications packet.

66. A combination, comprising:

a telephone headset adapter base for coupling a telephone headset to a telephone system, and including a digital interface bus adapted for coupling at least one accessory to the digital interface bus in order to transmit data packets between the telephone headset adapter base and the accessory, thereby allowing the telephone headset adapter base to control and monitor operations of the accessory; and

a communications protocol defining a packet structure for the data packets transmitted between the telephone headset adapter base and the accessory, via the interface bus, the communications protocol including at least one command for controlling an operation of the accessory or monitoring the status of the accessory.

67. The combination of claim 66, wherein the at least one command is selected from the group of commands consisting of:

a command for simulating operations as if a button, switch or dial on the accessory has been activated;

a command for simulating operations as if a button, switch or dial on the headset adapter base has been activated;

a command for resetting the accessory;

a command for determining the status of the accessory;

a command for reading from or writing to a memory structure within the accessory;

a command for determining the identity of the accessory; and

a command for requesting a firmware version number from the accessory.

68. The combination of claim 66, wherein the communications protocol further comprises:

a synch pulse having a rate bit which defines a speed at which the data packet is transmitted;

a source address byte which represents a bus address where the data packet was transmitted from; and

a destination address byte which represents a bus address where the data packet is being transmitted.

69. The combination of claim 66, wherein the communications protocol further comprises a checksum for detecting errors in transmission of the data packet.

70. A headset adapter base for testing a headset accessory coupled to the adapter base, the adapter base comprising:

a micro-controller, and

an interface bus coupled to the micro-controller and adapted to coupled to the headset accessory for transmitting and receiving communications packets back and forth between the micro-controller and the headset accessory in order to test the headset accessory and verify proper operation of the headset accessory.

71. The adapter base of claim 70, wherein the interface bus includes at least one bi-directional signaling which is used for transmitting and receiving the communications packets between the headset accessory and micro-controller.

72. The adapter base of claim 70, wherein each communications packet includes a synch pulse which defines a transmission rate for the communications packet.

73. The adapter base of claim 72, wherein the synch pulse includes a rate bit having a bit period which defines the transmission rate for the communications packet.

74. The adapter base of claim 73, wherein the rate bit includes a rising edge and a falling edge within the bit period, and further wherein a duration of time between the rising edge and the falling edge is used to determine the bit period which is inversely related to the transmission rate of the communications packet.

75. A method for testing a headset accessory comprising:

coupling the headset accessory to a headset adapter base having an accessory interface bus and a micro-controller;

transmitting and receiving communications packets back and forth between the micro-controller and the headset accessory in order to test the headset accessory and verify proper operation of the headset accessory.

76. The method of claim 75, wherein the interface bus includes at least one bi-directional signaling which is used for transmitting and receiving the communications packets between the headset accessory and micro-controller.

77. The method of claim 75, wherein each communications packet includes a synch pulse which defines a transmission rate for the communications packet.

78. The method of claim 77, wherein the synch pulse includes a rate bit having a bit period which defines the transmission rate for the communications packet.

79. The method of claim 78, wherein the rate bit includes a rising edge and a falling edge within the bit period, and further wherein a duration of time between the rising edge and the falling edge is used to determine the bit period which is inversely related to the transmission rate of the communications packet.